



ON Semiconductor®

<http://onsemi.com>

STK534U342C-E

Advance Information

Inverter IPM for 3-phase Motor Drive

Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP). Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers.
- Built-in cross conduction prevention.
- Externally accessible embedded thermistor for substrate temperature measurement

Certification

- UL1557 (File number: E339285).

Specifications

Absolute Maximum Ratings at Tc = 25°C

| Parameter | Symbol | Remarks | Ratings | Unit |
|----------------------------|--------------------|---|-------------|------|
| Supply voltage | V _{CC} | P to U-, V-, W-, surge<500V *1 | 450 | V |
| Collector-emitter voltage | V _{CE} | P to U, V, W or U, V, W, to U-, V-, W- | 600 | V |
| Output current | I _o | P,U-,V-,W-,U,V,W terminal current | ±5 | A |
| | | P,U-,V-,W-,U,V,W terminal current, Tc=100°C | ±3 | A |
| Output peak current | I _{op} | P,U-,V-,W-,U,V,W terminal current, P.W.=1ms | ±10 | A |
| Pre-driver voltage | VD1,2,3,4 | VB1 to U, VB2 to V, VB3 to W, VDD to VSS *2 | 20 | V |
| Input signal voltage | V _{IN} | HIN1, 2, 3, LIN1, 2, 3 | -0.3 to VDD | V |
| FLTEN terminal voltage | V _{FLTEN} | FLTEN terminal | -0.3 to VDD | V |
| Maximum power dissipation | P _d | IGBT per 1 channel | 27.7 | W |
| Junction temperature | T _j | IGBT, FRD, Pre-Driver IC | 150 | °C |
| Storage temperature | T _{stg} | | -40 to +125 | °C |
| Operating case temperature | T _c | H-IC case | -20 to +100 | °C |
| Tightening torque | | A screw part *3 | 0.9 | Nm |
| Withstand voltage | V _{is} | 50Hz sine wave AC 1 minute *4 | 2000 | VRMS |

Reference voltage is “V_{SS}” terminal voltage unless otherwise specified.

*1: Surge voltage developed by the switching operation due to the wiring inductance between P and U-(V-, W-) terminal.

*2: Terminal voltage: VD1=VB1-U, VD2=VB2-V, VD3=VB3-W, VD4= V_{DD}-V_{SS}.

*3: Flatness of the heat-sink should be 0.15mm and below.

*4: Test conditions : AC2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

STK534U342C-E

Electrical Characteristics at $T_c = 25^\circ\text{C}$, VD1, VD2, VD3, VD4 = 15V

| Parameter | Symbol | Conditions | Test circuit | MIN | TYP | MAX | Unit |
|--|-------------------|---|--------------|------|------|------|--------------------|
| Power output section | | | | | | | |
| Collector-emitter cut-off current | I_{CE} | $V_{CE} = 600\text{V}$ | Fig.1 | - | - | 100 | μA |
| Bootstrap diode reverse current | $I_{R(BD)}$ | $V_{R(BD)} = 600\text{V}$ | | - | - | 100 | μA |
| Collector to emitter saturation voltage | $V_{CE(SAT)}$ | $I_o = 5\text{A}, T_j = 25^\circ\text{C}$ | Fig.2 | - | 1.6 | 2.4 | V |
| | | $I_o = 3\text{A}, T_j = 100^\circ\text{C}$ | | - | 1.4 | - | |
| Diode forward voltage | V_F | $I_o = -5\text{A}, T_j = 25^\circ\text{C}$ | Fig.3 | - | 1.2 | 1.8 | V |
| | | $I_o = -3\text{A}, T_j = 100^\circ\text{C}$ | | - | 1.0 | - | |
| Junction to case thermal resistance | $\theta_{j-c(T)}$ | IGBT | - | - | - | 4.5 | $^\circ\text{C/W}$ |
| | $\theta_{j-c(D)}$ | FWD | | - | - | 6 | |
| Control (Pre-driver) section | | | | | | | |
| Pre-driver power dissipation | ID | VD1,2,3 = 15V | Fig.4 | - | 0.08 | 0.4 | mA |
| | | VD4 = 15V | | - | 1.6 | 4 | |
| High level Input voltage | Vin H | HIN1,HIN2,HIN3, | - | 2.5 | - | - | V |
| Low level Input voltage | Vin L | LIN1,LIN2,LIN3 to V_{SS} | - | - | - | 0.8 | V |
| Logic 1 input leakage current | I_{IN+} | VIN=+3.3V | - | - | 100 | 143 | μA |
| Logic 0 input leakage current | I_{IN-} | VIN=0V | - | - | - | 2 | μA |
| FLTEN terminal sink current | I_{oSD} | FAULT:ON / VFLTEN=0.1V | - | - | 2 | - | mA |
| FLTEN clearance delay time | FLTCLR | From time fault condition clear | - | 1.0 | 2.0 | 3.0 | ms |
| FLTEN Threshold | VEN+ | VEN rising | - | - | - | 2.5 | V |
| | VEN- | VEN falling | - | 0.8 | - | - | V |
| ITRIP threshold voltage | VITRIP | ITRIP(16) to $V_{SS}(29)$ | - | 0.44 | 0.49 | 0.54 | V |
| ITRIP to shutdown propagation delay | t_{ITRIP} | | - | 340 | 550 | 800 | ns |
| ITRIP blanking time | $t_{ITRIPBL}$ | | - | 250 | 350 | - | ns |
| V_{CC} and V_{BS} supply undervoltage protection reset | V_{CCUV+} | | - | 10.5 | 11.1 | 11.7 | V |
| | V_{BSUV+} | | | | | | |
| V_{CC} and V_{BS} supply undervoltage protection set | V_{CCUV-} | | - | 10.3 | 10.9 | 11.5 | V |
| | V_{BSUV-} | | | | | | |
| V_{CC} and V_{BS} supply undervoltage hysteresis | V_{CCUVH} | | - | 0.14 | 0.2 | - | V |
| | V_{BSUVH} | | | | | | |

Reference voltage is " V_{SS} " terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

STK534U342C-E

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15V, VCC=300V, L=3.9mH

| Parameter | Symbol | Conditions | Test circuit | MIN | TYP | MAX | Unit |
|------------------------------------|--------|-------------------------------------|--------------|--------------|-----|-----|------|
| Switching Character | | | | | | | |
| Switching time | t ON | Io = 5A | Fig.5 | 0.3 | 0.5 | 1.2 | μs |
| | t OFF | | | - | 1.5 | 2.0 | |
| Turn-on switching loss | Eon | Io=3A | Fig.5 | - | 170 | - | μJ |
| Turn-off switching loss | Eoff | | | - | 60 | - | μJ |
| Total switching loss | Etot | | | - | 230 | - | μJ |
| Turn-on switching loss | Eon | Io=3A, Tc=100°C | Fig.5 | - | 190 | - | μJ |
| Turn-off switching loss | Eoff | | | - | 80 | - | μJ |
| Total switching loss | Etot | | | - | 270 | - | μJ |
| Diode reverse recovery energy | Erec | If=3A, P=400V, L=0.5mH, Tc=100°C | - | - | 14 | - | μJ |
| Diode reverse recovery time | Trr | | - | - | 57 | - | ns |
| Reverse bias safe operating area | RBSOA | Io =10A, VCE = 450V | - | Full square- | | | |
| Short circuit safe operating area | SCSOA | VCE = 400V, Tc=100°C | - | 4 | - | - | μs |
| Allowable offset voltage slew rate | dv/dt | Between U,V,W to U-,V-,W- | - | -50 | - | 50 | V/ns |

Reference voltage is “VSS” terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes

- When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch. After protection operation ends, it returns automatically within about typ. 2ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO: with hysteresis about 0.2V) is as follows.

Upper side:

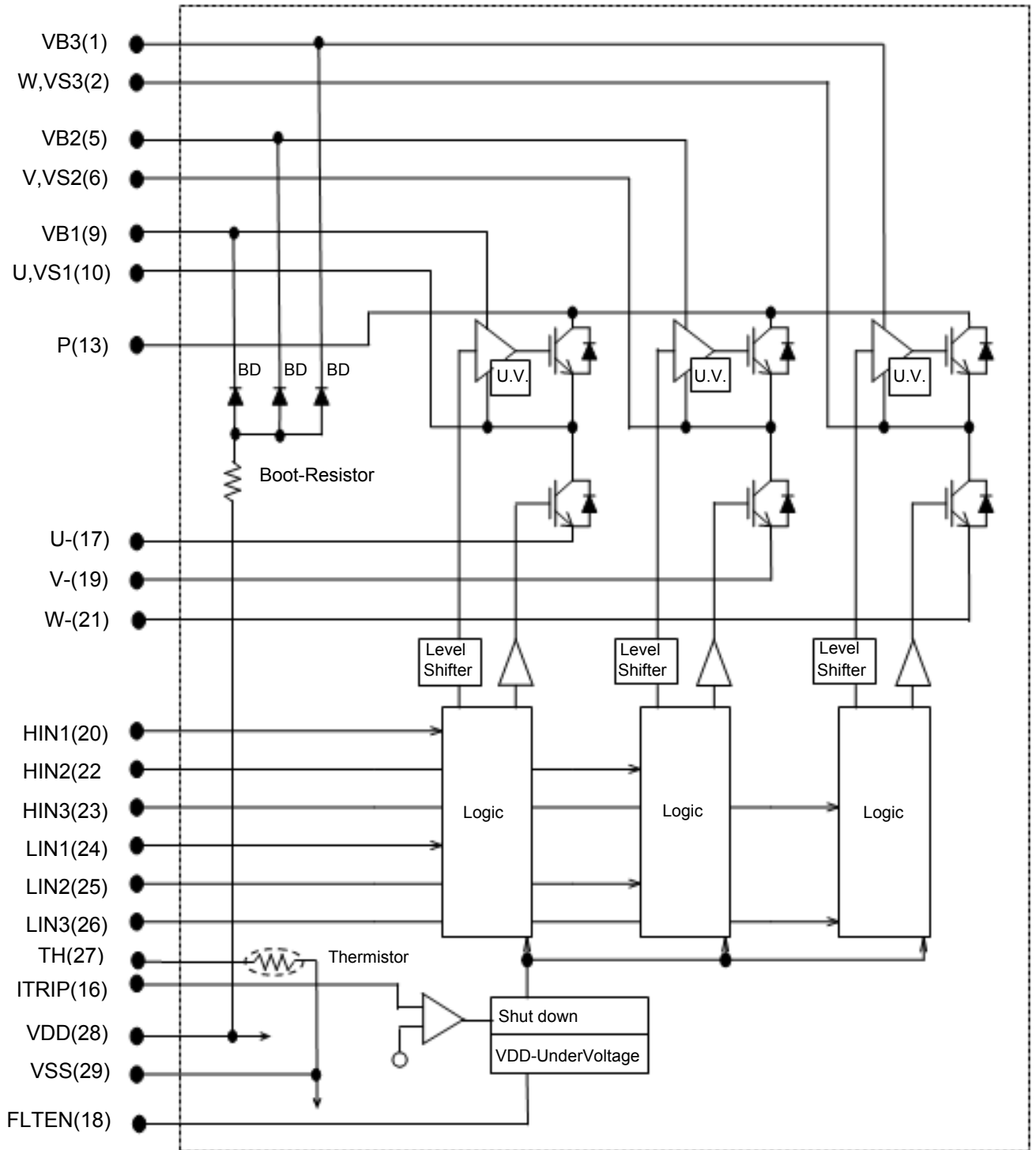
The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.

Lower side:

The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

- When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.6 Nm to 0.9 Nm.
- When use the over-current protection with external resistor, please set resistance value so that current protection value becomes equal to or less than the double (2 times) of the rating output electric current (Io).

Equivalent Block Diagram



Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ ICE / IR(BD)

| | | | | | | |
|---|----|----|----|----|----|----|
| | U+ | V+ | W+ | U- | V- | W- |
| M | 13 | 13 | 13 | 10 | 6 | 2 |
| N | 10 | 6 | 2 | 17 | 19 | 21 |

| | | | |
|---|-------|-------|-------|
| | U(BD) | V(BD) | W(BD) |
| M | 9 | 5 | 1 |
| N | 29 | 29 | 29 |

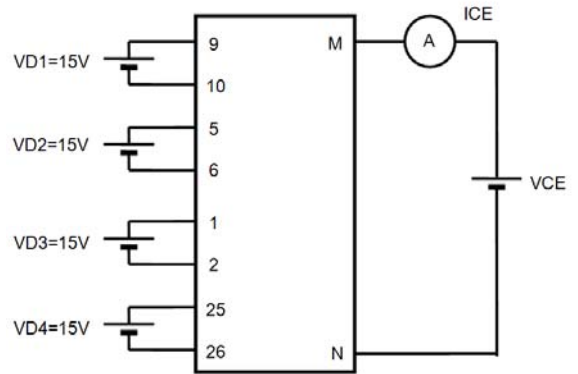


Fig.1

■ VCE(SAT) (Test by pulse)

| | | | | | | |
|---|----|----|----|----|----|----|
| | U+ | V+ | W+ | U- | V- | W- |
| M | 13 | 13 | 13 | 10 | 6 | 2 |
| N | 10 | 6 | 2 | 17 | 19 | 21 |
| m | 20 | 22 | 23 | 24 | 25 | 26 |

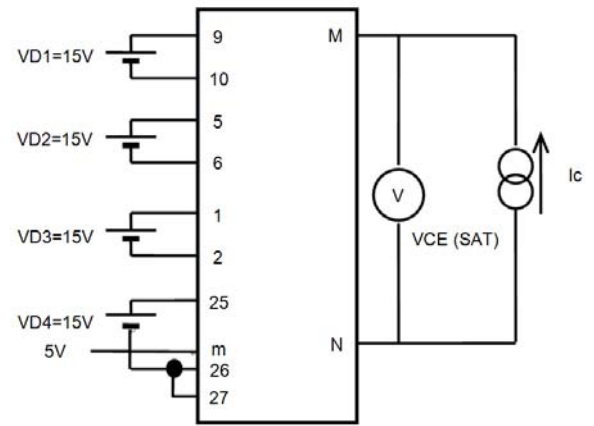


Fig.2

■ VF (Test by pulse)

| | | | | | | |
|---|----|----|----|----|----|----|
| | U+ | V+ | W+ | U- | V- | W- |
| M | 13 | 13 | 13 | 10 | 6 | 2 |
| N | 10 | 6 | 2 | 17 | 19 | 21 |

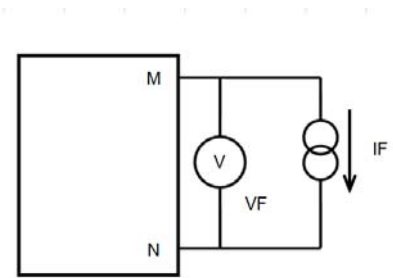


Fig.3

■ ID

| | | | | |
|---|-----|-----|-----|-----|
| | VD1 | VD2 | VD3 | VD4 |
| M | 9 | 5 | 1 | 28 |
| N | 10 | 6 | 2 | 29 |

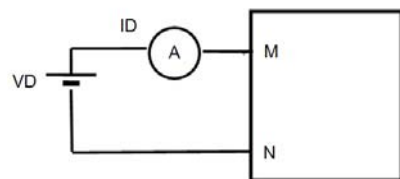


Fig.4

■ Switching time (The circuit is a representative example of the lower side U phase.)

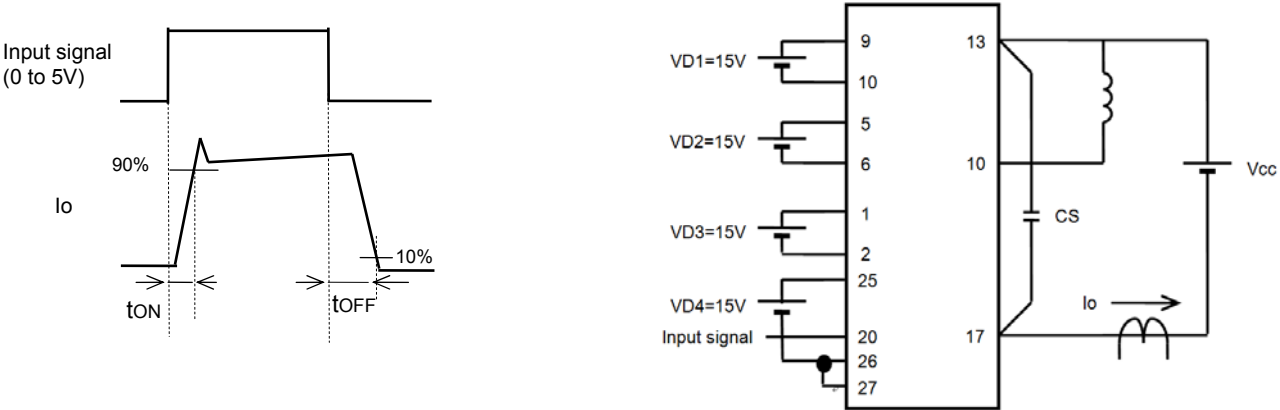


Fig.5

Input / Output Timing Chart

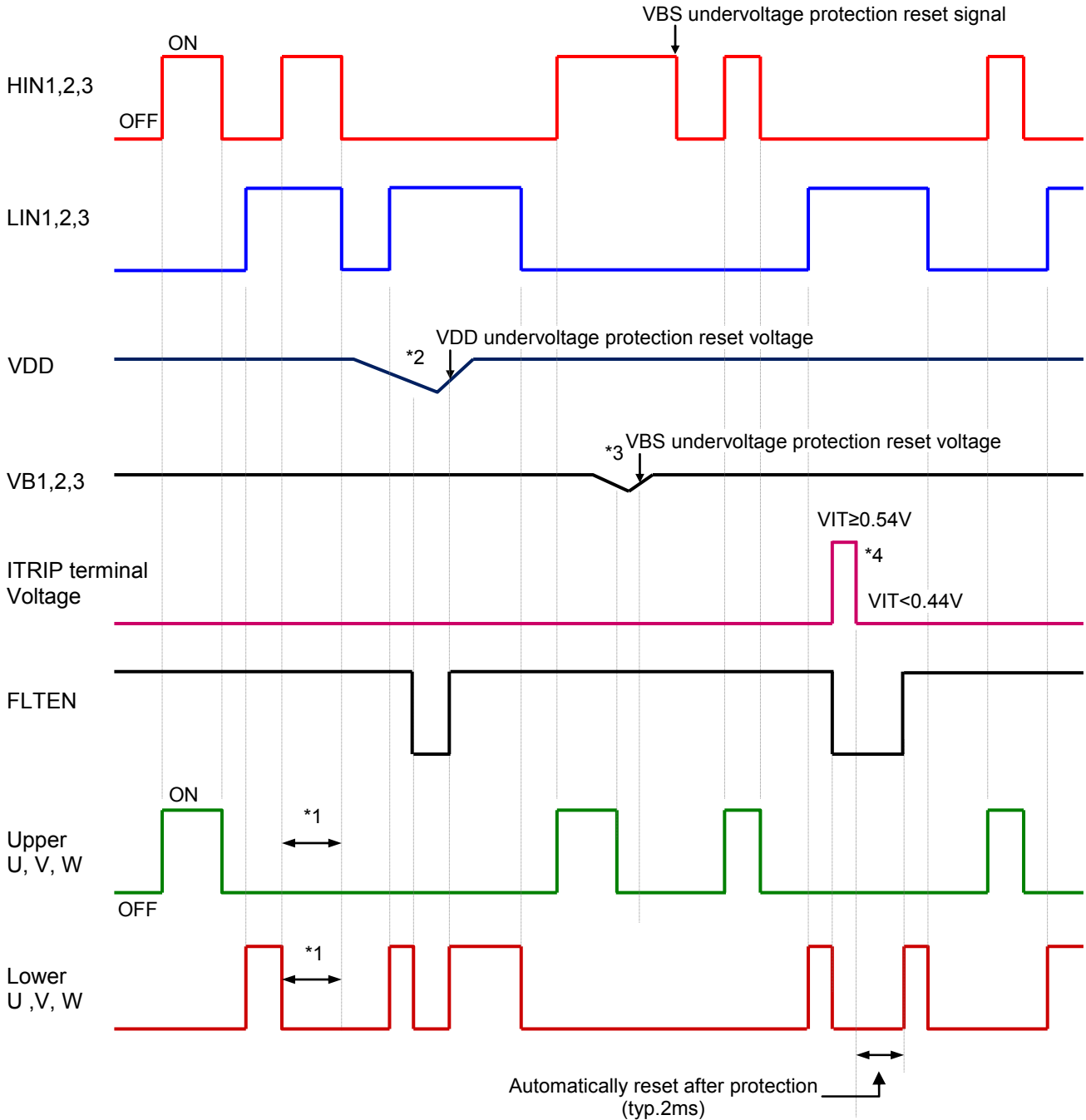
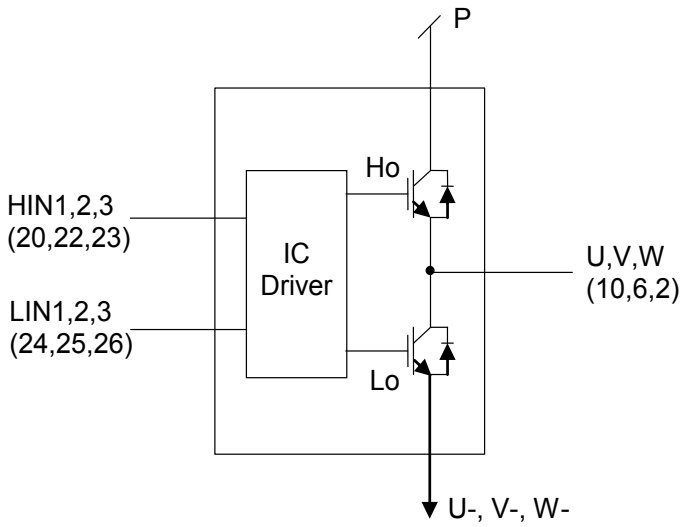


Fig. 7

Notes

- *1 shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.
- *2 when V_{DD} decreases all gate output signals will go low and cut off all 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
- *3 when the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- *4 when V_{ITRIP} exceeds threshold all IGBT's are turned off and normal operation resumes 2ms (typ) after over current condition is removed.

Logic level table



| INPUT | | | OUTPUT | | | |
|-------|-----|-------|--------|----|----------------|-------|
| HIN | LIN | Itrip | Ho | Lo | U,V,W | FLTEN |
| H | L | L | H | L | P | OFF |
| L | H | L | L | H | U-,V-,W- | OFF |
| L | L | L | L | L | High Impedance | OFF |
| H | H | L | L | L | High Impedance | OFF |
| X | X | H | L | L | High Impedance | ON |

Fig. 8

Sample Application Circuit

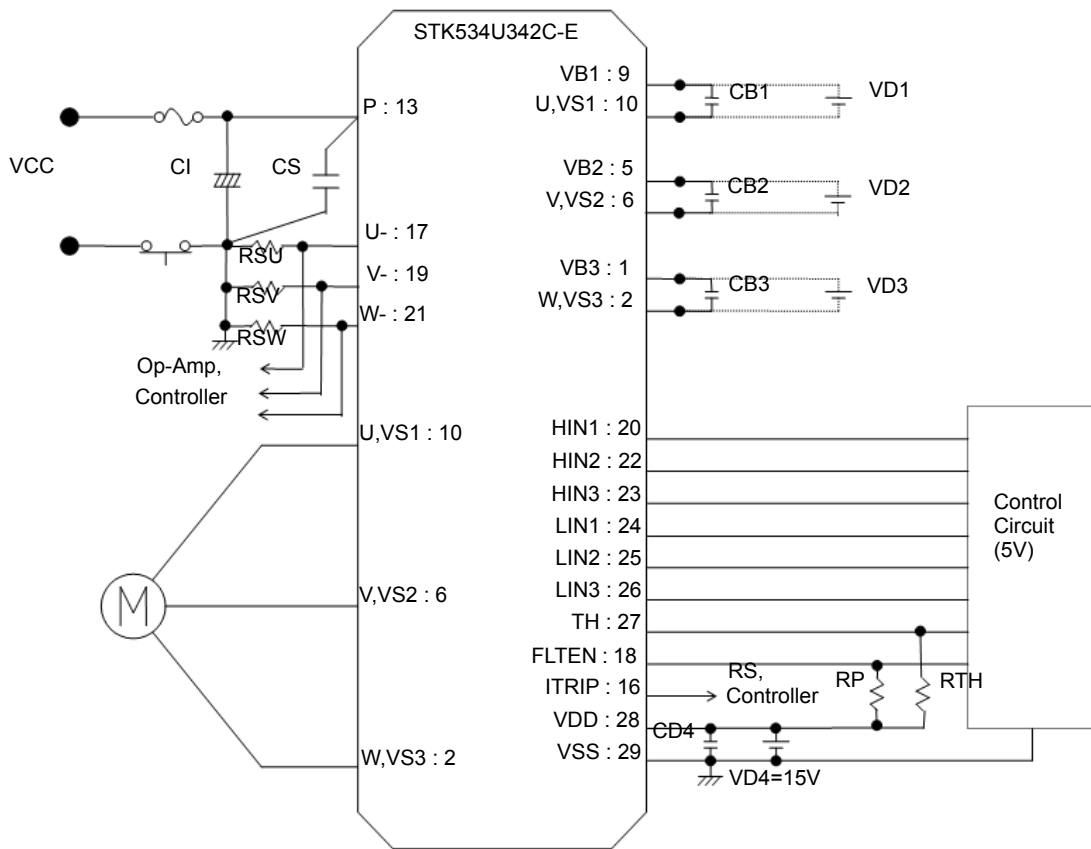


Fig.9

STK534U342C-E

Recommended Operating Condition at $T_c = 25^\circ\text{C}$

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|----------------|--------------------------------|------|------|------|---------------|
| Supply voltage | V_{CC} | + to U-(V-,W-) | 0 | 280 | 450 | V |
| Pre-driver supply voltage | $VD_{1,2,3}$ | VB1 to U,VB2 to V,VB3 to W | 12.5 | 15 | 17.5 | V |
| | VD_4 | V_{DD} to V_{SS} *1 | 13.5 | 15 | 16.5 | |
| ON-state input voltage | V_{IN} (ON) | HIN1,HIN2,HIN3, | 3.0 | - | 5.0 | V |
| OFF-state input voltage | V_{IN} (OFF) | LIN1,LIN2,LIN3 | 0 | - | 0.3 | |
| PWM frequency | fPWM | | 1 | - | 20 | kHz |
| Dead time | DT | Turn-off to turn-on (external) | 2.5 | - | - | μs |
| Allowable input pulse width | PWIN | ON and OFF | 1 | - | - | μs |
| Mounting torque | | 'M3' type screw | 0.6 | - | 0.9 | Nm |

*1 Pre-drive power supply ($VD_4=15\pm 1.5\text{V}$) must be have the capacity of $I_o=20\text{mA}$ (DC), 0.5A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes bootstrap diode and resistor. Therefore, by adding a capacitor (CB : about 1 to 47 μ F), a single power supply drive is enabled. In this case, an electric charge is charged to "CB" by making lower side IGBT turn on.
And, please select the capacitance of "CB"(externally set) equal to or less than 47 μ F(\pm 20%).If selecting the capacitance more than 47 μ F(\pm 20%), connect a resistor(about 20 Ω)in series between each 3-phase upper side power supply terminals(VB1,2,3) and each bootstrap capacitor. Also, the upper side power supply voltage sometimes declines by the way of controlling. Please confirm the voltage with an actual set.
(When not using the bootstrap circuit, each upper side pre-drive power supply needs an external independent power supply.)
 2. Because the jump voltage which is accompanied by the vibration in case of switching operation occurs by the influence of the floating inductance of the wiring of the outer power supply which is connected with of the "+" terminal and the "U-"("V-", "W-") terminal, restrains and spares serge voltage being as the connection of the snubber circuit (Capacitor / CS /about 0.1 μ F to 10 μ F) for the voltage absorption with the neighborhood as possible between the "+" and the point of intersection of the "U-", "V-" and "W-" terminal, and so on, with making a wiring length (among the terminals each from "CI")short and making a wiring inductance small.
 3. The "FLTEN" terminal (18pin) is open Drain (It is operating as "FLTEN" when becoming Low). This terminal serves as the shut down function of the built-in pre-driver. (When the terminal voltage is above 3V,normalcy works, and it is shut down when it is equal to or less than 0.8V.) Please make pulling up outside so that "FLTEN" terminal voltages become more than 3V. When the pull up voltage (VP) is at 5V, pull up resistor (RP) connects above 6.8k Ω , and in case of VP=15V, RP connects above 20k Ω .
 4. Inside the IPM, thermistor is connected to between the "TH" terminal (27pin) and the "VSS" terminal (29pin). The thermistor can be used as the temperature monitor by pull up with the resistance (Rth).
(This is for temperature monitors, and it is not a thing having the hyper temperature protection function by IPM oneself). This is for temperature monitors of substrate in the steady movement state. Therefore, please take care of the suddenly and partial fever.
 5. The pull-down resistor (:33k Ω (typ)) is connected with the inside of the signal input terminal, but please connect the pull-down resistor(about 2.2 to 3.3k Ω) outside to decrease the influence of the noise by wiring etc.
 6. The overcurrent protection feature operates only when it is possible to do a circuit control normally. For safety, recommend installation a fuse, and so on in the "VCC" line.
 7. Because the IPM can be destroyed when the motor connection terminal (pins 2, 6, and 10) is opened while the motor is running, please be especially careful of the connection (soldering condition) of this terminal.
 8. The "ITRIP" terminal (16pin) is the input terminal of the built-in comparator. It can stop movement by inputting the voltage more than Vref (0.44V to 0.54V). (At the time of movement, usually give me it for the voltage less than Vref).
Please use it as various protections such as the overcurrent protection (feedback from external shunt resistance).
In addition, the protection movement is not done a latch of.
After the protection movement end, I become the movement return state after typ.2ms. Therefore, please do the protection movement detection of all input signals in OFF (LOW) promptly afterward.
 9. When input pulse width is less than 1 μ s, an output may not react to the pulse. (Both ON signal and OFF signal)
- This data shows the example of the application circuit and does not guarantee a design as the mass production set.

The characteristic of thermistor

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|-------------------------|-----------|-----------|------|------|------|------|
| Resistance | R_{25} | T = 25°C | 97 | 100 | 1034 | kΩ |
| Resistance | R_{125} | T = 125°C | 4.93 | 5.38 | 5.88 | kΩ |
| B-Constant (25 to 50°C) | B | | 4165 | 4250 | 4335 | k |
| Temperature Range | | | -40 | | +125 | °C |

■ This data shows the example of the application circuit, does not guarantee a design as the mass production set.

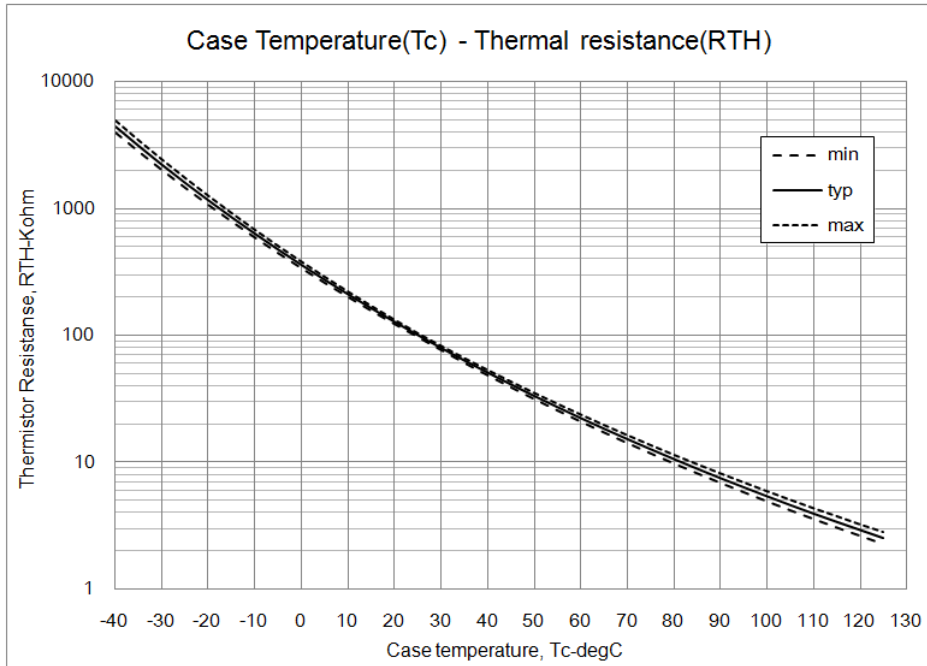


Fig.10 Variation of thermistor resistance with temperature

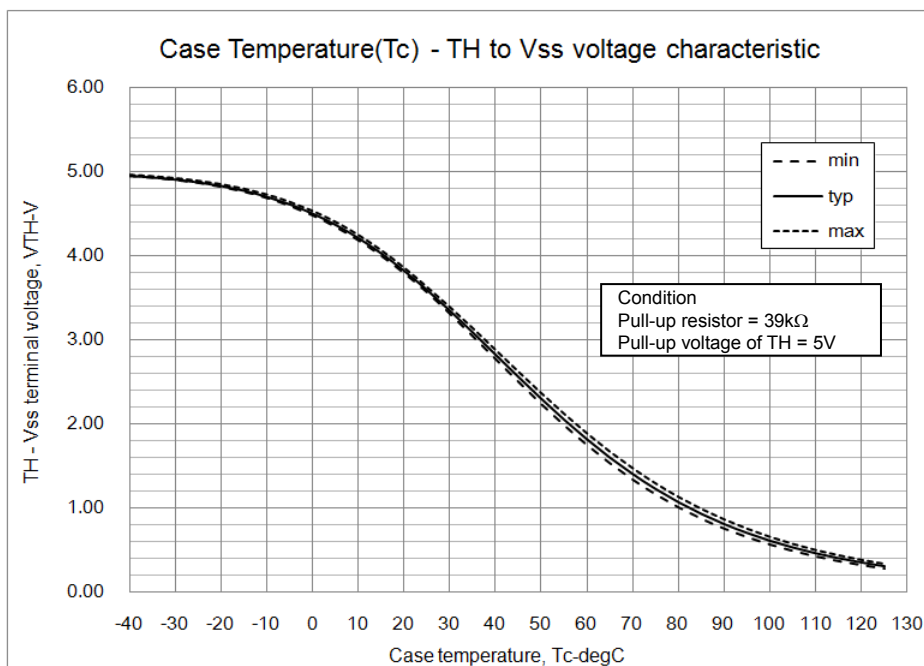


Fig.11 Variation of temperature sense voltage with thermistor temperature

The characteristic of PWM switching frequency

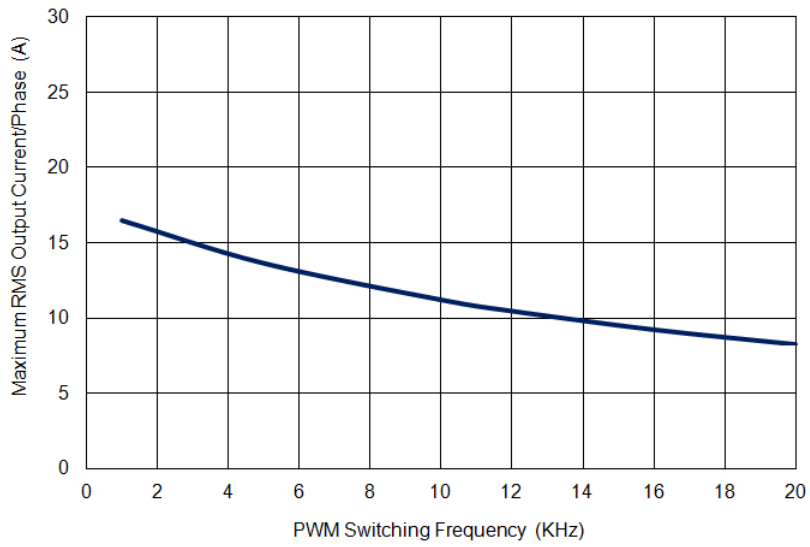


Fig.12 Maximum sinusoidal phase current as function of switching frequency at $T_c=100^{\circ}\text{C}$, $V_{CC}=300\text{V}$

Switching waveform

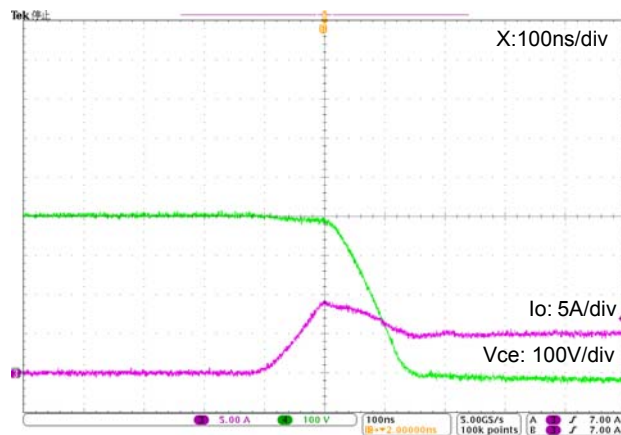


Fig. 13 IGBT Turn-on. Typical turn-on waveform at $T_c=100^{\circ}\text{C}$, $V_{CC}=400\text{V}$, $I_o=5\text{A}$

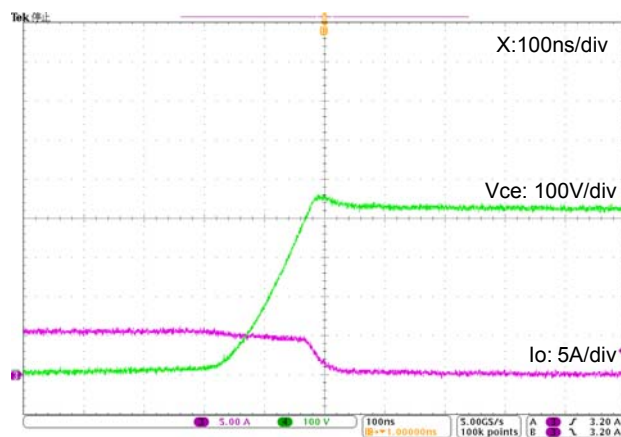


Fig. 14 IGBT Turn-off. Typical turn-off waveform $T_c=100^{\circ}\text{C}$, $V_{CC}=400\text{V}$, $I_o=5\text{A}$

CB capacitor value calculation for bootstrap circuit

Calculate condition

| Item | Symbol | Value | Unit |
|--|--------|-------|------|
| Upper side power supply. | VBS | 15 | V |
| Total gate charge of output power IGBT at 15V. | Qg | 45 | nC |
| Upper side power supply low voltage protection. | UVLO | 12 | V |
| Upper side power dissipation. | IDMAX | 400 | μA |
| ON time required for CB voltage to fall from 15V to UVLO | TONMAX | - | s |

Capacitance calculation formula

Tonmax is upper arm maximum on time equal the time when the CB voltage falls from 15V to the upper limit of Low voltage protection level.

“ton-maximum” of upper side is the time that CB decreases 15V to the maximum low voltage protection of the upper side (12V).

Thus, CB is calculated by the following formula.

$$VBS * CB - Qg - IDMAX * TONMAX = UVLO * CB$$

$$CB = (Qg + IDMAX * TONMAX) / (VBS - UVLO)$$

The relationship between tonmax and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of Cb is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

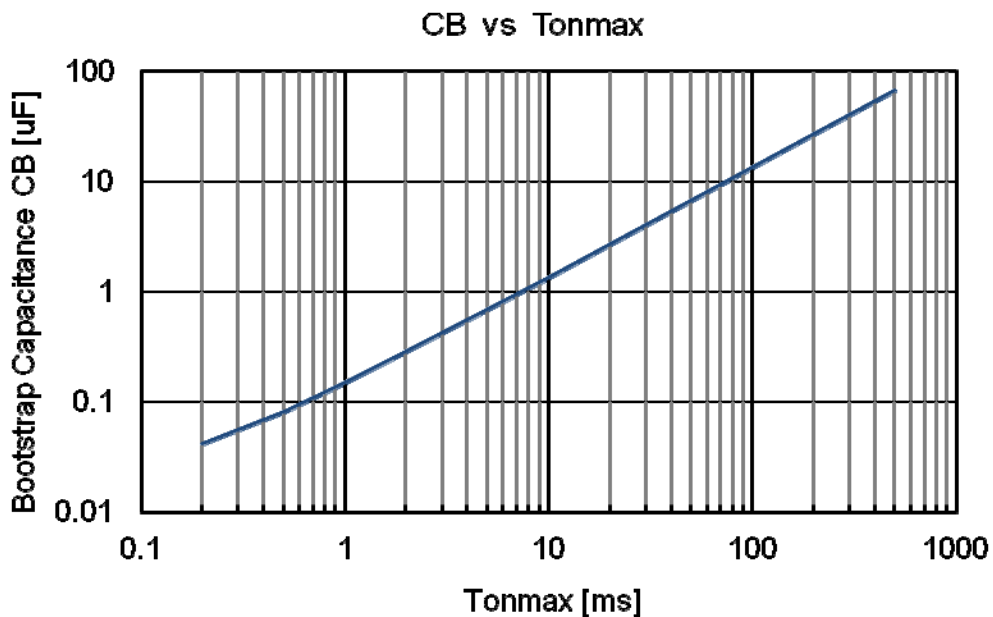


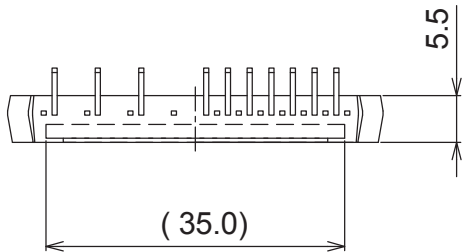
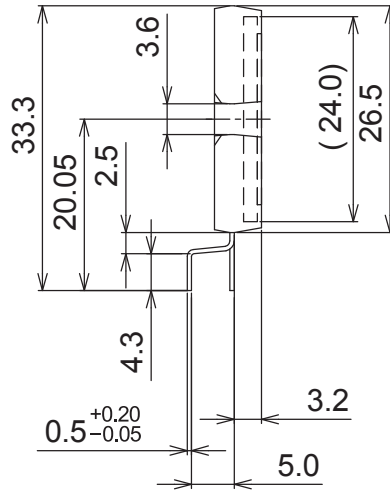
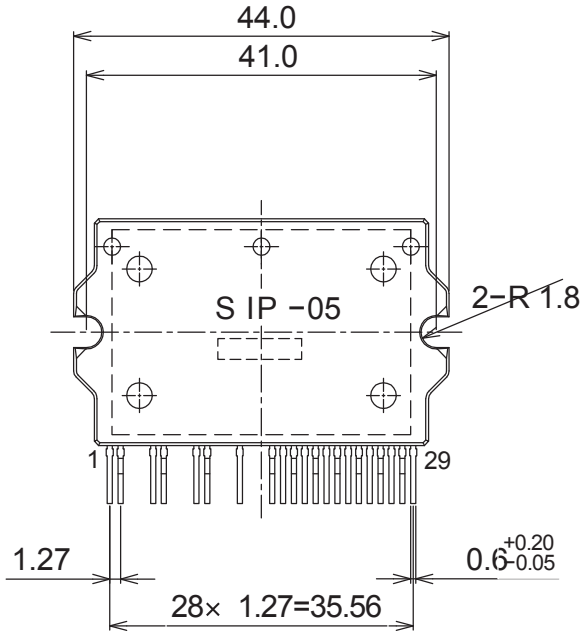
Fig.15 TONMAX vs CB characteristic

Package Dimensions

unit : mm

SIP29 44x26.5
CASE 127CJ
ISSUE O

missing pin : 3, 4, 7, 8, 11, 12, 14, 15



ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|----------------------------|--------------------------|
| STK534U342C-E | SIP29 44x26.5 (Pb-Free) | 11 / Tube |

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.